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18ELD14

First Semester M.Tech. Degree Examination, Dec.2018/Jan.2019
Digital Circuits and Logic Design

Time: 3 hrs. Max. Marks: 100

Note: ***Answer FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Find the function $f(x_1, x_2, x_3, x_4)$ for the threshold network shown in Fig.Q1(a). Show the map. **(06 Marks)**

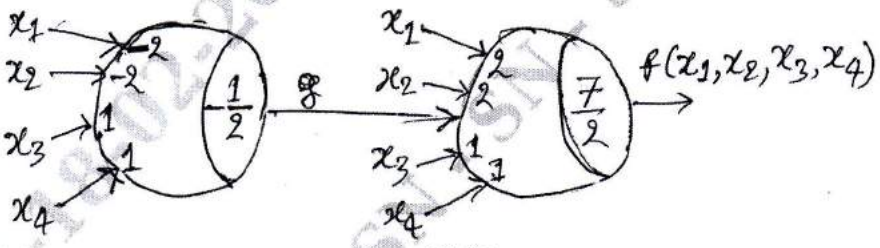

Fig.Q1(a)

b. Explain the elementary properties. **(04 Marks)**

c. Given the switching function :
$f(x_1, x_2, x_3, x_4) = \Sigma(2, 3, 6, 7, 10, 12, 14, 15)$
Find a minimal threshold logic realization. **(10 Marks)**

OR

2 a. Explain the concept of threshold logic and its physical realization. **(10 Marks)**

b. Determine whether the function :
$f(x_1, x_2, x_3, x_4) = \Sigma(0, 1, 3, 4, 5, 6, 7, 12, 13)$
is a threshold function and if it is, find a weight–threshold vector. **(10 Marks)**

Module-2

3 a. Explain with an example a fault detection by path sensitizing method. **(10 Marks)**

b. i) Find all the static hazards in the circuit shown in Fig.Q3(b). Assume the individual elements to be hazard free.

ii) Changing only the parameters of the threshold element, redesign the circuit so that all static hazards are eliminated. **(10 Marks)**

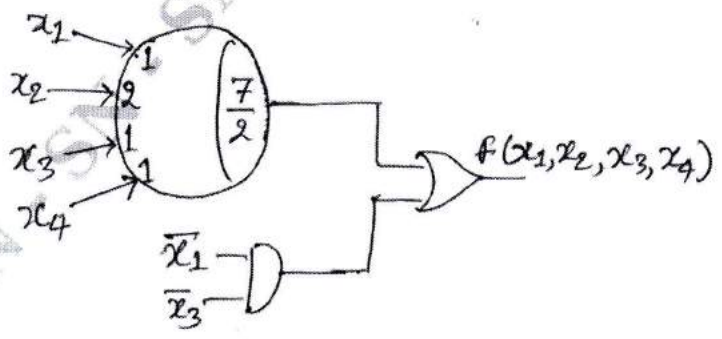

Fig.Q3(b)

OR

4 a. Explain the static hazard and hazard free circuits, with example. **(10 Marks)**

b. Find the minimal sets of fault-detection test for AND-OR network function 'f',

$f(w, x, y, z) = \bar{w}\,\bar{y} + \bar{y}\,z + wxz + xy\,\bar{z}$. **(10 Marks)**

Module-3

5 a. Find the equivalence partition for the machine shown in Table Q5(a).

i) Show the standard form of the corresponding reduced machine

ii) Find a minimum length sequence that distinguishes state A from state B. **(10 Marks)**

PS	NS, Z	
	X = 0	X = 1
A	B, 1	H, 1
B	F, 1	D, 1
C	D, 0	E, 1
D	C, 0	F, 1
E	D, 1	C, 1
f	C, 1	C, 1
G	C, 1	D, 1
H	C, 0	A, 1

TableQ5(a)

b. Draw the merger graph and its minimal form for the machine in Table Q5(b). Also write its merger table. **(10 Marks)**

PS	NS, Z			
	I_1	I_2	I_3	I_4
A	–	C, 1	E, 1	B, 1
B	E, 0	–	–	–
C	F, 0	F, 1	–	–
D	–	–	B, 1	–
E	–	F, 0	A, 0	D, 1
F	C, 0	–	B, 0	C, 1

Table.Q5(b)

OR

6 a. For incompletely specified machine shown in Table.Q6(a). Find the minimum state reduced machine containing the original one using merger graph, and compatibility graph. **(10 Marks)**

PS	NS, Z		
	I_1	I_2	I_3
A	C, 0	E, 1	–
B	C, 0	E, –	–
C	B, –	C, 0	A, –
D	B, 0	C, –	E, –
E	–	E, 0	A, –

Table.Q6(a)

b. Apply Boolean difference method to test wire 'h' in the circuit shown in Fig.Q6(b).

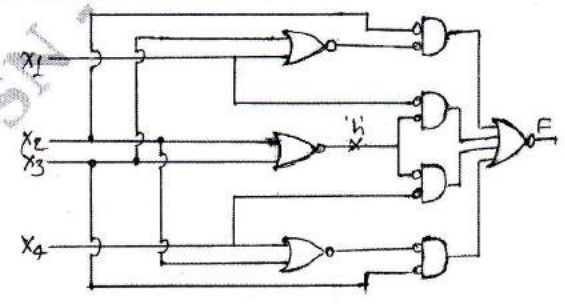

Fig. Q6(b) **(10 Marks)**

Module-4

7 The machine shown in Table. Q7 has the following output consistent and input consistent partitions :

$\lambda_0 = \{\overline{A,E,F};\ \overline{B,D};\ \overline{C,G}\}$

$\lambda_i = \{\overline{A,E,F};\ \overline{B,C,D,G}\}$

i) List all other closed partitions

ii) Use state splitting to decompose the machine into components which operate in parallel.

PS	NS		Output, Z	
	x = 0	x = 1	x = 0	x = 1
A	B	C	0	0
B	A	F	1	1
C	F	E	1	0
D	F	E	1	1
E	G	D	0	0
F	D	B	0	0
G	E	F	1	0

Table. Q7 **(20 Marks)**

OR

8 a. For the machine given in Table. Q8(a), determine the π-Lattice. **(10 Marks)**

PS	NS	
	x = 0	x = 1
A	E	B
B	E	A
C	D	A
D	C	F
E	F	C
F	E	C

Table. Q8(a)

b. Explain :

i) Input – consistent

ii) Output consistent

iii) Closed partitions. **(10 Marks)**

Module-5

9 a. Explain the Homing experiments with example. **(10 Marks)**

b. Explain the adaptive distinguishing experiment by considering the machine shown in Table.Q9(b). **(10 Marks)**

PS	NS, Z	
	x = 0	x = 1
A	C, 0	A, 1
B	D, 0	C, 1
C	B, 1	D, 1
D	C, 1	A, 0

Table.Q9(b)

OR

10 a. Find the shortest Homing sequence and the shortest synchronizing sequenced for the machine shown in Table. Q10(a). **(10 Marks)**

PS	NS, Z	
	x = 0	x = 1
A	A, 1	E, 0
B	A, 0	C, 0
C	B, 0	D, 1
D	C, 1	C, 0
E	C, 0	D, 0

Table. Q10(a)

b. Explain the different steps involving in machine identification with the help of following data :

Time	$t_1 - t_2$	$t_2 - t_3$	$t_3 - t_4$	$t_4 - t_5$	$t_5 - t_6$	$t_6 - t_7$	$t_7 - t_8$
Input sequence	1	1	1	0	1	0	1
Output sequence	0	1	0	0	1	0	0

(10 Marks)

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